Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10796499	ESPOSITO, BEN
	Examiner	Art Unit
	Alrobaye, Idriss N	2183

SEARCHED

Class	Subclass	Date	Examiner
712	35	01-10-2007	IA
712	19	4/18/2008	IA
710	52	4/18/2008	IA
370	371, 291	9/23/2008	IA
708	301	9/23/2008	IA
377	76	9/24/2008	IA

SEARCH NOTES

Search Notes	Date	Examiner
Inventor Search (double patenting)	01-10-2007	IA
See East Search history	01-10-2007	IA
NPL (google; terms used: array register column multiplexer or mux, matrix row registers, dsp or digital signal processing, tap or tapped delay line or delay circuit)	01-11-2007	IA
Consulted WQAS Mano with regards to the final action, even though a first final action was sent	05/01/2008	IA
See East search history	4/18/2008	IA
Consulted primary Rich	9/23/2008	IA
See East search history	9/23/2008	IA
Inventor search for double patenting (PALM)	9/25/2008	IA
NPL(Google, ACM, google scholar, terms used: shift register architecture; tap delay circuit; structure of shift register; Parallel operation linear feedback shift register; linear feedback shift register; folded delay line; folded delay line and shift registers; tapped delay line and column of registers; tap delay line and column of registers)	9/24/2008	IA

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
712	35, 19 class and text search	9/24/2008	IA
370	291, 371 class and text search	9/24/2008	IA
710	52 class and text search	9/24/2008	IA
708	301 class and text search	9/24/2008	IA
377	76 class and text search	9/24/2008	IA